We claim:

1. A first type very long instruction word (VLIW) memory (VIM) direct memory access (DMA) apparatus comprising:

a single VLIW memory (VIM) for storing a plurality of instruction words;

a DMA interface;

a DMA very long instruction word (VLIW) line buffer; and

a single cycle write VLIW line controller which controls the loading of multiple instruction words into VIM during a single VIM DMA request.

2. The apparatus of claim 1 wherein the VIM is a two port memory allowing simultaneous read and write accesses.

3. The apparatus of claim 2 wherein said controller provides each of the two ports its own address and read or write control signals.

4. The apparatus of claim 1 wherein said line buffer receives and temporarily stores a data packet comprising a load/modify VLIW memory address (LV1) instruction and a plurality of short instruction words (SIWs) constituting a VLIW to be loaded at an address specified in the LV1 instruction.

5. The apparatus of claim 1 wherein said controller provides cycle borrow control to the DMA interface.

6. A second type very long instruction word (VLIW) memory (VIM) direct memory access (DMA) apparatus comprising:

a partitioned VLIW memory (VIM) having a separate VIM section per VLIW slot function unit;

a DMA interface;

a DMA very long instruction word (VLIW) line buffer; and

a VIM load controller for separately controlling the loading of each separate VIM section.

7. The apparatus of claim 6 wherein each separate VIM section has two ports allowing simultaneous read and write accesses.

8. The apparatus of claim 6 wherein said line buffer receives and temporarily stores a data packet comprising a load/modify VLIW memory address (LV2) instruction and a plurality of short instruction words (SIWs) constituting a specified functional VIM portion to be loaded at an address specified in the LV2 instruction.

9. A first type of method for providing very long instruction word (VLIW) memory (VIM) direct memory access (DMA), said method comprising the steps of:

storing a DMA very long instruction word (VLIW) line buffer;

utilizing a single cycle write VLIW line controller which controls the loading of multiple instruction words during a single VIM DMA request to control the loading of a single VLIW memory (VIM) for storing a plurality of instruction words; and

selectively routing the VLIW from said line buffer to said VIM on a DMA interface.

10. The method of claim 9 wherein the VIM is a two port memory allowing simultaneous read and write accesses, and the method further comprises the step of providing each of the two ports its own address and read or write control signals.

11. The method of claim 9 further comprising the step of receiving and temporarily storing in said line buffer a plurality of data packets comprising a load/modify VLIW memory address (LV1) instruction and a plurality of short instruction words (SIWs) constituting a VLIW to be loaded at an address specified in the LV1 instruction.

12. The method of claim 9 further comprising the step of utilizing said controller to provide cycle borrow control to the DMA interface.

13. A second type of method for providing very long instruction word (VLIW) memory (VIM) direct memory access (DMA), said method comprising the steps of:

storing a DMA very long instruction word (VLIW) line buffer;

utilizing a VIM load controller for separately controlling the loading of each separate VIM section in a partitioned VLIW memory (VIM) having a separate VIM section per VLIW slot function unit; and

selectively routing the appropriate portions of said VLIW from said line buffer to said separate VIM sections on a DMA interface.

14. The method of claim 13 wherein each separate VIM section has two ports allowing simultaneous read and write accesses, and the method further comprises the step of separately providing each of the two parts for each separate VIM section its open address and read or write control signals.

15. The method of claim 13 further comprising the step of receiving and temporarily storing in said line buffer a plurality of data packets comprising a load/modify VLIW memory address (LV2) instruction and a plurality of short instruction words (SIWs) constituting a specified functional VIM portion to be loaded at an address specified in the LV2 instruction.

16. A VIM loading apparatus consisting of DMA facilities to DMA VLIW instructions into PE and/or SP data memory; VIM load instructions that utilize VLIW load slot that cause the VLIW instruction stored in PE and/or SP data memory to be readout of PE and/or SP data memory and loaded into VIM.